S7885 Touch Controller Datasheet

PN: 505-000610-01 Rev. B

Introduction

The Synaptics® S7885 is a high performance touchscreen controller for the automotive market. The controller has 102 sensing channels for use in touchscreens up to 14.5 inches (diagonal) with a 16:10 aspect ratio and a sensor pitch of 5 mm. The maximum number of nodes is 2,405 (for example, a configuration of 63 RX x 39 TX or 65 RX x 37 TX).

General description

The S7885 supports self-capacitance, mutual-capacitance, and hybrid sensing with up to 10-finger detection. Fast report rates (up to 150 Hz) and flexible sensing frequency from 50 to 500 kHz are also supported.

The S7885 provides high performance hardware filtering for noise mitigation, moisture detection, and severe common mode noise rejection. The device also offers a high-performance on-chip charge pump, patented Synaptics SignalClarity™ driving schemes, and advanced firmware algorithms. Finally, the device has patented display synchronization technology that eliminates display noise from horizontal refresh.

Features and benefits

- ISO-TS16949 compliant
- AEC-Q100 qualification to Automotive Grade 2 (–40ºC to 105ºC)
- Production Part Approval Process (PPAP) documentation
- 176LQFP (20 mm x 20 mm x 1.6 mm)
- Glove detection
- Moisture mitigation
- Proximity support
- Gesture support
- Thick lens support (4.5 mm at a dielectric constant of 8)
- Curved lens designs with maximum thickness same as thick lens support with any minimum thickness
- Power modes:
  - Touch active
  - Normal operation
  - Sensor sleep
- Serial interfaces:
  - I^2C (100/400 kHz)
  - SPI slave
- Power supply schemes:
  - 2.7V to 3.6V supply voltage
  - Internal positive and negative charge pumps for increased TX voltage
- Best-in-class capacitance sensing:
  - Up to 10-finger detection and simultaneous tracking
  - 102 sensing channels with positional interpolation providing best-in-class accuracy and resolution
  - Optimum SNR performance
- In-system reprogrammability (reflash) support
- Internal power-on reset detector
- Hardware filtering for noise mitigation
- Supports configurable frequency shifting
- Supports advanced sensor/display architecture including:
  - Touch controller on sensor FPC tail
  - Touch controller on main board
  - Sensor ITO pattern on lens (OGS)
- On-Cell sensor designs
- Built-in self-test feature
- Self-calibrating — no host side calibration needed
- Fully compatible with Synaptics Design Studio™ 5 tool chain for production-ready touch sensing development

Contents

Architecture

The S7885 is a fully self-contained, ready-to-use, capacitance-sensing system on a chip (SoC). Synaptics proprietary microcontroller and firmware handle all calibration, capacitance-sensing, computation of finger position, and gesture reporting.

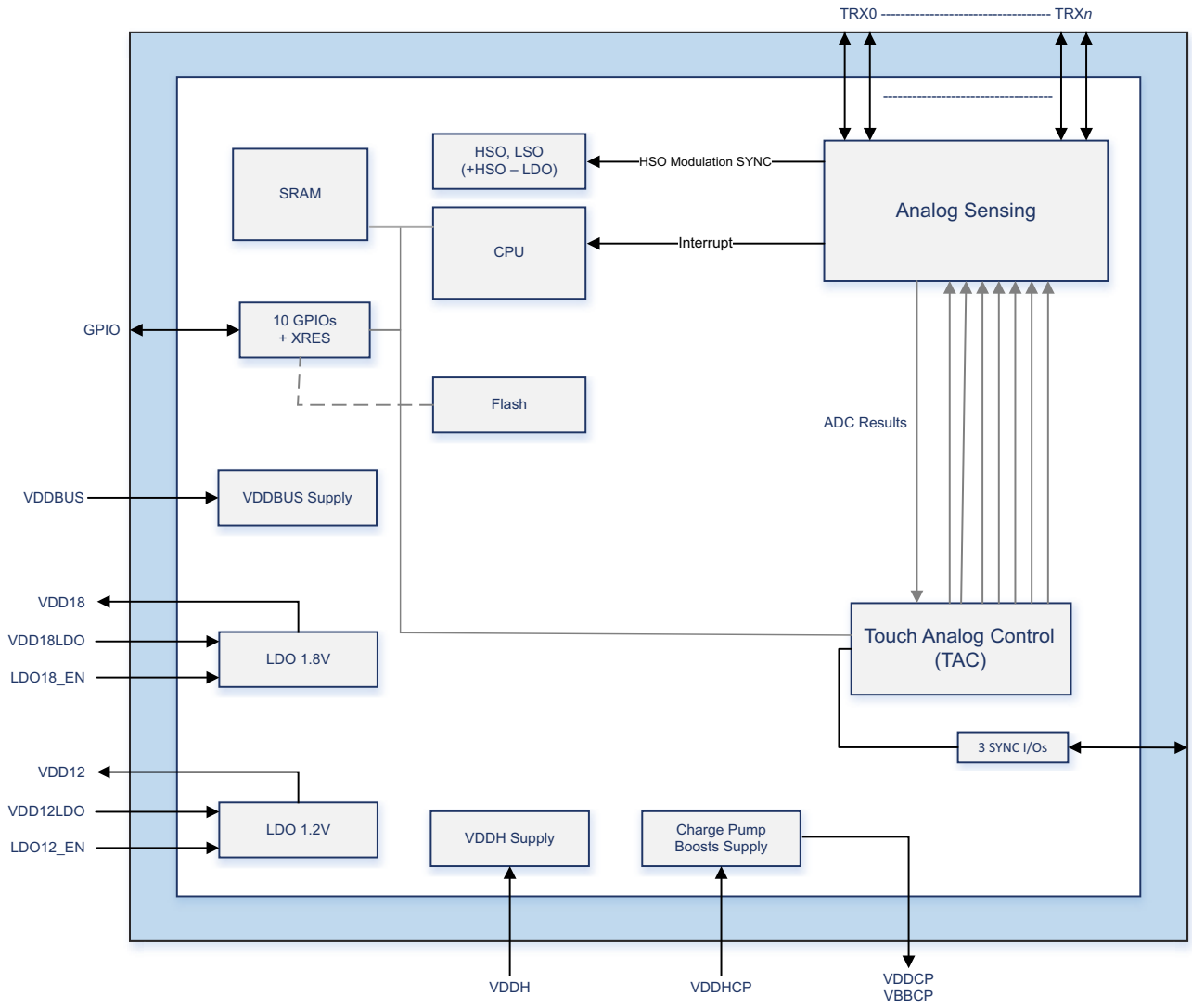

Figure 1. S7885 block diagram

Pin assignments

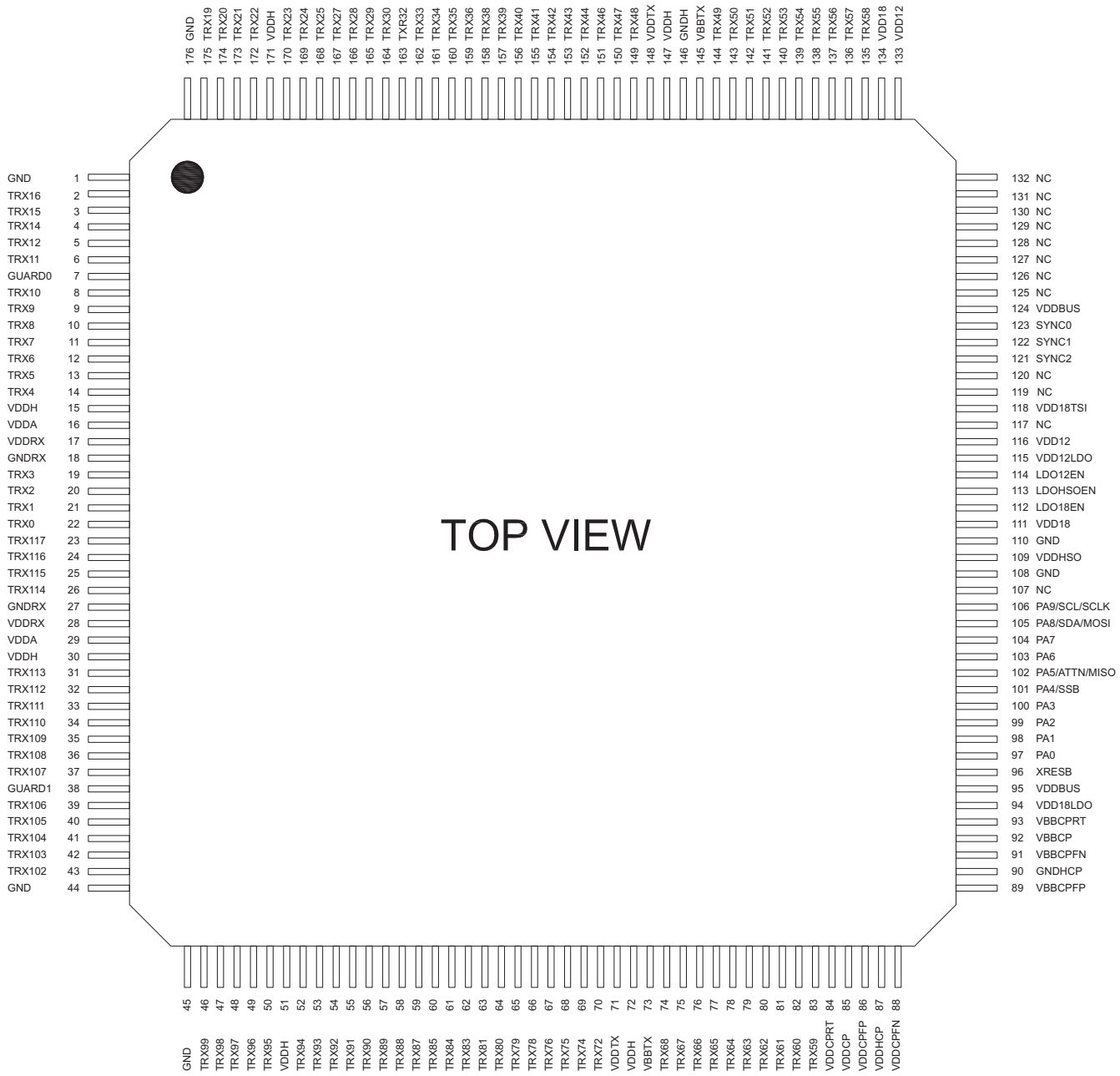

Figure 2. S7885 176LQFP pin assignments (top view)

Pin definitions

Table 1. S7885 176LQFP pin definitions

Pin Location	Signal	Pin Type	Description
1	GND	Ground	Analog ground.
2	TRX16	I/O	Transmitter or receiver electrode, configurable in bank 1 grouping.
3	TRX15	I/O	Transmitter or receiver electrode, configurable in bank 1 grouping.
4	TRX14	I/O	Transmitter or receiver electrode, configurable in bank 1 grouping.
5	TRX12	I/O	Transmitter or receiver electrode, configurable in bank 1 grouping.
6	TRX11	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
7	GUARD0	O	Guard amplifier 0 output.
8	TRX10	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
9	TRX9	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
10	TRX8	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
11	TRX7	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
12	TRX6	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
13	TRX5	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
14	TRX4	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
15	VDDH	Power	External 3.3V power input.
16	VDDA	Filter Pin	Low-pass filtered version of VDDH used by charge integrators.
17	VDDRX	Filter Pin	Low-pass filtered version of VDDH.
18	GNDRX	Ground	Filtered analog ground.
19	TRX3	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
20	TRX2	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
21	TRX1	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
22	TRX0	I/O	Transmitter or receiver electrode, configurable in bank 0 grouping.
23	TRX117	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
24	TRX116	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
25	TRX115	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
26	TRX114	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
27	GNDRX	Ground	Filtered analog ground.
28	VDDRX	Filter Pin	Low-pass filtered version of VDDH.
29	VDDA	Filter Pin	Low-pass filtered version of VDDH used by charge integrators.
30	VDDH	Power	External 3.3V power input.

Table 1. S7885 176LQFP pin definitions (Continued)

Pin Location	Signal	Pin Type	Description
31	TRX113	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
32	TRX112	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
33	TRX111	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
34	TRX110	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
35	TRX109	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
36	TRX108	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
37	TRX107	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
38	GUARD1	O	Guard amplifier 1 output.
39	TRX106	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
40	TRX105	I/O	Transmitter or receiver electrode, configurable in bank 9 grouping.
41	TRX104	I/O	Transmitter or receiver electrode, configurable in bank 8 grouping.
42	TRX103	I/O	Transmitter or receiver electrode, configurable in bank 8 grouping.
43	TRX102	I/O	Transmitter or receiver electrode, configurable in bank 8 grouping.
44	GND	Ground	Analog ground.
45	GND	Ground	Analog ground.
46	TRX99	I/O	Transmitter or receiver electrode, configurable in bank 8 grouping.
47	TRX98	I/O	Transmitter or receiver electrode, configurable in bank 8 grouping.
48	TRX97	I/O	Transmitter or receiver electrode, configurable in bank 8 grouping.
49	TRX96	I/O	Transmitter or receiver electrode, configurable in bank 8 grouping.
50	TRX95	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
51	VDDH	Power	External 3.3V power input.
52	TRX94	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
53	TRX93	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
54	TRX92	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
55	TRX91	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
56	TRX90	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
57	TRX89	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
58	TRX88	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
59	TRX87	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
60	TRX85	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
61	TRX84	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.

Table 1. S7885 176LQFP pin definitions (Continued)

Pin Location	Signal	Pin Type	Description
62	TRX83	I/O	Transmitter or receiver electrode, configurable in bank 7 grouping.
63	TRX81	I/O	Transmitter or receiver electrode, configurable in bank 6 grouping.
64	TRX80	I/O	Transmitter or receiver electrode, configurable in bank 6 grouping.
65	TRX79	I/O	Transmitter or receiver electrode, configurable in bank 6 grouping.
66	TRX78	I/O	Transmitter or receiver electrode, configurable in bank 6 grouping.
67	TRX76	I/O	Transmitter or receiver electrode, configurable in bank 6 grouping.
68	TRX75	I/O	Transmitter or receiver electrode, configurable in bank 6 grouping.
69	TRX74	I/O	Transmitter or receiver electrode, configurable in bank 6 grouping.
70	TRX72	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
71	VDDTX	Power	Internal power, connect to pin 148.
72	VDDH	Power	External 3.3V power input.
73	VBBTX	Power	Internal power, connect to pin 145.
74	TRX68	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
75	TRX67	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
76	TRX66	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
77	TRX65	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
78	TRX64	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
79	TRX63	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
80	TRX62	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
81	TRX61	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
82	TRX60	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
83	TRX59	I/O	Transmitter or receiver electrode, configurable in bank 5 grouping.
84	VDDCPRT	Power	Power input to the positive charge pump bypass switch (typically connected to positive charge pump).
85	VDDCP	Power	Output of positive charge pump (external voltage should never be applied)
86	VDDCPFP	Analog	Positive charge pump capacitor, positive side.
87	VDDHCP	Power	External 3V power input to internal charge pumps.
88	VDDCPFN	Analog	Positive charge pump capacitor, negative side.
89	VBBCPFP	Analog	Negative charge pump capacitor, positive side.
90	GNDHCP	Ground	Charge pump GND.
91	VBBCPFN	Analog	Negative charge pump capacitor, negative side.

Table 1. S7885 176LQFP pin definitions (Continued)

Pin Location	Signal	Pin Type	Description
92	VBBCP	Power	Output of negative charge pump.
93	VBBCPRT	Power	Power input to the negative charge pump bypass switch (typically connected to negative charge pump).
94	VDD18LDO	Power	Connect to VDDH.
95	VDDBUS	Power	Connect to VDDH. Power supply for all GPIO pins.
96	XRESB	I	Dedicated active low reset pin; has internal pull-up to VDDBUS.
97	PA0	GPIO	Spare GPIO.
98	PA1	GPIO	Spare GPIO.
99	PA2	GPIO	Spare GPIO.
100	PA3	GPIO	Spare GPIO.
101	PA4/SSB	GPIO	Spare GPIO; SPI SSB.
102	PA5/ATTN/MISO	GPIO	I^2C ATTN interrupt; SPI MISO.
103	PA6	GPIO	Spare GPIO.
104	PA7	GPIO	Spare GPIO.
105	PA8/SDA/MOSI	GPIO	I^2C data (SDA); alternate SPI MOSI; true open drain I/O.
106	PA9/SCL/SCLK	GPIO	I^2C clock (SCL); alternate SPI CLK; true open drain I/O.
107	NC	No Connect	Do not connect.
108	GND	Ground	Analog ground.
109	VDDHSO	Power	HSO/LDO power supply pin; do not connect.
110	GND	Ground	Analog ground.
111	VDD18	Power	Output of internal 1.8V LDO.
112	LDO18EN	I	Connect to VDDH.
113	LDOHSOEN	Test	Always connect to VDD18 (pin 111).
114	LDO12EN	I	Connect to VDD18 (pin 111).
115	VDD12LDO	Power	Connect to VDD18 (pin 111).
116	VDD12	Power	Output of internal 1.2V LDO.
117	NC	No Connect	Do not connect.
118	VDD18TSI	Power	Connect to VDD18 (pin 111).
119	NC	No Connect	Do not connect.
120	NC	No Connect	Do not connect.
121	SYNC2	I/O	Multi-chip synchronization signal.

Table 1. S7885 176LQFP pin definitions (Continued)

Pin Location	Signal	Pin Type	Description
122	SYNC1	I/O	Multi-chip synchronization signal.
123	SYNC0	I/O	Multi-chip synchronization signal.
124	VDDBUS	Power	Connect to VDDH. Power supply for all GPIO pins.
125	NC	No Connect	Do not connect.
126	NC	No Connect	Do not connect.
127	NC	No Connect	Do not connect.
128	NC	No Connect	Do not connect.
129	NC	No Connect	Do not connect.
130	NC	No Connect	Do not connect.
131	NC	No Connect	Do not connect.
132	NC	No Connect	Do not connect.
133	VDD12	Power	Output of internal 1.2V LDO.
134	VDD18	Power	Output of internal 1.8V LDO.
135	TRX58	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
136	TRX57	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
137	TRX56	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
138	TRX55	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
139	TRX54	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
140	TRX53	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
141	TRX52	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
142	TRX51	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
143	TRX50	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
144	TRX49	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
145	VBBTX	Power	Internal power, connect to pin 73.
146	GNDH	Ground	Package digital ground.
147	VDDH	Power	External 3.3V power input.
148	VDDTX	Power	Internal power, connect to pin 71.
149	TRX48	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
150	TRX47	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
151	TRX46	I/O	Transmitter or receiver electrode, configurable in bank 4 grouping.
152	TRX44	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.

Table 1. S7885 176LQFP pin definitions (Continued)

Pin Location	Signal	Pin Type	Description
153	TRX43	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.
154	TRX42	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.
155	TRX41	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.
156	TRX40	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.
157	TRX39	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.
158	TRX38	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.
159	TRX36	I/O	Transmitter or receiver electrode, configurable in bank 3 grouping.
160	TRX35	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
161	TRX34	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
162	TRX33	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
163	TXR32	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
164	TRX30	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
165	TRX29	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
166	TRX28	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
167	TRX27	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
168	TRX25	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
169	TRX24	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
170	TRX23	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
171	VDDH	Power	External 3.3V power input.
172	TRX22	I/O	Transmitter or receiver electrode, configurable in bank 2 grouping.
173	TRX21	I/O	Transmitter or receiver electrode, configurable in bank 1 grouping.
174	TRX20	I/O	Transmitter or receiver electrode, configurable in bank 1 grouping.
175	TRX19	I/O	Transmitter or receiver electrode, configurable in bank 1 grouping.
176	GND	Ground	Analog ground.

Transmitter and receiver configurations

Table 2. S7885 transmitter and receiver bank options

Bank	TRX	Number of TRX
0	TRX0 to TRX12	13
1	TRX14 to TRX16, TRX19 to 21	6
2	TRX22 to TRX25, TRX27 to TRX30, TRX32 to TRX35	12
3	TRX36, TRX38 to TRX44	8
4	TRX46 to TRX58	13
5	TRX59 to TRX68, TRX72	11
6	TRX74 to TRX76, TRX78 to TRX81	7
7	TRX83 to TRX85, TRX87 to TRX95	12
8	TRX96 to TRX99, TRX102 to TRX104	7
9	TRX105 to TRX117	13

Configuration pin options

Table 3. S7885 axis setting options

Bank	Axis Setting			
	0	1	2	3
0	13R	13R	13R	13R
1	6R	6R	6T	6T
2	12R	12T	12R	12T
3	8T	8T	8R	8R
4	13T	13R	13T	13R
5	11T	11R	11T	11R
6	7T	7T	7R	7R
7	12R	12T	12R	12T
8	7R	7R	7T	7T
9	13R	13R	13R	13R
Total	63R; 39T	63R; 39T	65R; 37T	65R; 37T

Sample schematic

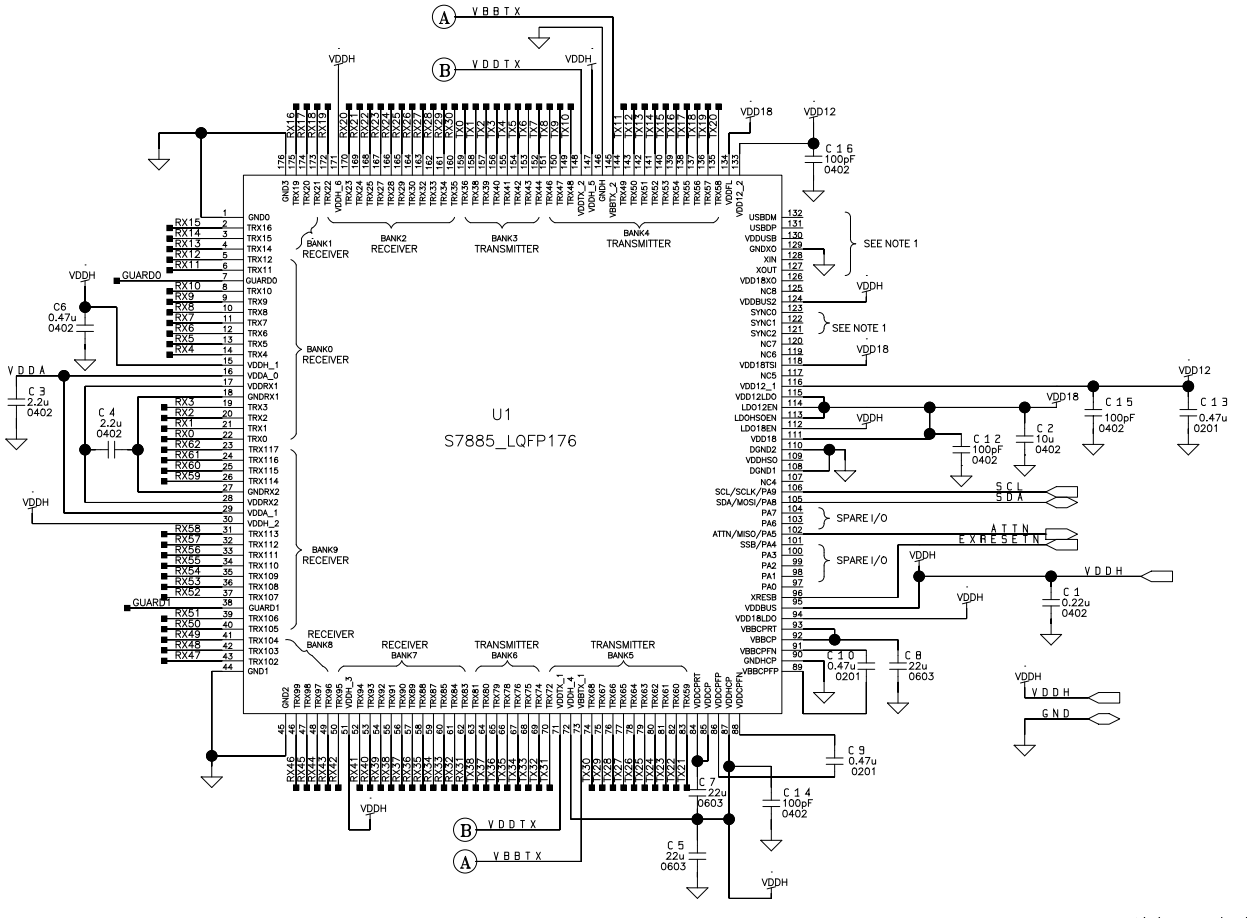

Figure 3. S7885 sample I²C schematic with a single power supply VDDH only

Note 1: Leave unused pins unconnected.

Note 2: This is a sample schematic for an AXIS_SENSE = 0; configuration: 63 RX and 39 TX; single power RMI over I²C (VDDH).

Note 3: Place capacitors as close to power supply pins as possible.

Sample schematic parts designator

The component values shown in the following table are typical values suitable for most applications. However, each system design has different requirements that may require different component values to better match that system. Please consult your Synaptics FAE if you have special system design requirements beyond those outlined in this datasheet.

Table 4. S7885 sample schematic part designators

Designator	Description
C1	CAPACITOR, 0.22 UF, X5R, 10%, 10V, 0402
C2	CAPACITOR, 10 UF, X5R, 20%, 6.3V, 0402
C3	CAPACITOR, 2.2 UF, X5R, 20%, 6.3V, 0402
C4	CAPACITOR, 2.2 UF, X5R, 20%, 6.3V, 0402
C5	CAPACITOR, 22 UF, X5R, 20%, 6.3V, 0603
C6	CAPACITOR, 0.47 UF, X5R, 20%, 6.3V, 0402
C7	CAPACITOR, 22 UF, X5R, 20%, 6.3V, 0603
C8	CAPACITOR, 22 UF, X5R, 20%, 6.3V, 0603
C9	CAPACITOR, 0.47 UF, X5R, 20%, 6.3V, 0201
C10	CAPACITOR, 0.47 UF, X5R, 20%, 6.3V, 0201
C12	CAPACITOR, 100 PF, C0G, 5%, 50V, 0402
C13	CAPACITOR, 0.47 UF, X5R, 20%, 6.3V, 0201
C14	CAPACITOR, 100 PF, C0G, 5%, 50V, 0402
C15	CAPACITOR, 100 PF, C0G, 5%, 50V, 0402
C16	CAPACITOR, 100 PF, C0G, 5%, 50V, 0402

Power supply configuration

The S7885 is designed for a single external power supply rail. Table 5 provides the possible configuration.

For details on sensor/FPCA design and routing guidelines, refer to the *ClearPad Sensor Design Guidelines* (PN: 511-000384-01).

Table 5. S7885 power supply configuration

Configuration	VDD12	VDD18	VDDH	VDDBUS	LDO12EN	LDO18EN	Description
1	Internal	Internal	External	Connect to VDDH	Connect to VDD18	Connect to VDDH	External VDDH and VDDBUS Internal 1.8V, 1.2V

Note: The VDDBUS shares an external power supply with VDDH. VDDBUS must follow the VDDH power specification in Table 7.

Host interface

The S7885 is available with an I²C host interface. The host communicates with the S7885 by reading and writing 8-bit data registers. Full details of Synaptics interface protocols can be found in the *Synaptics RMI4 Specification* (PN: 511-000405-01).

Attention signal

In addition to standard I²C signals, the S7885 provides an attention output (ATTN) that is asserted to indicate that new data is available for reading by the host. The ATTN signal is intended to be used as an interrupt source to a host processor. ATTN functionality is added by user interface firmware so pin allocation, polarity and drive options (open-drain or push-pull) are defined at the time of firmware build. Operation of the ATTN signal is shown in Figure 4.

I²C interfacing

Connection

Figure 5 shows an example of host connection using the S7885 I²C interface. The values of the pull-up resistors should be chosen to ensure that the rise times of the SDA and SCL signals are within the limits set by the I²C specification. This depends on what other slave devices, if any, are on the I²C bus but typically would fall within the range of 2.2 kΩ –10 kΩ.

Refer to the *ClearPad Integration Guide* (PN: 511-000399-01) for additional information.

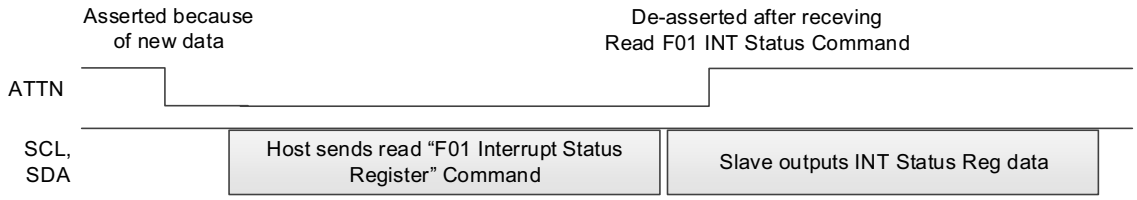

Figure 4. Attention line behavior (I²C interface shown)

Note: The attention line is also de-asserted when the host disables interrupts.

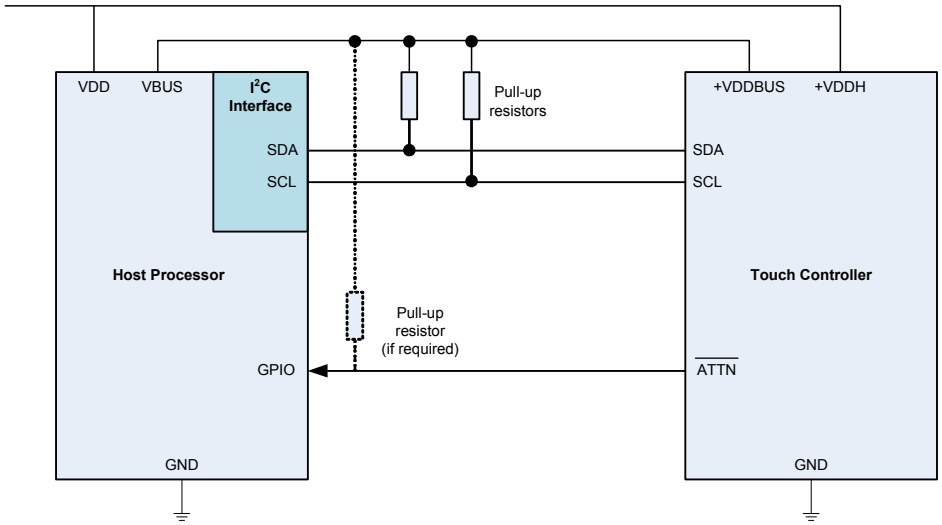

Figure 5. Typical connection of the touch controller to the host (I²C)

Clock stretching

Special attention should be paid to clock stretching when interfacing with a Synaptics touch controller over I^2C. The host processor must support clock stretching. The first byte of a transaction contains the slave address and read/write bit. At the end of the first byte, the touch controller holds SCL low (clock stretches) and checks that the slave address matches its own.

If the slave address does not match, the S7885 will not stretch the clock on subsequent byte transmissions until it detects the next start condition. If the slave address does match, the touch controller acknowledges and may stretch the clock after some or all of the subsequent bytes within the same transaction (Figure 6).

Note: Typical clock stretch time (Tcstr) is less than 25 µs.

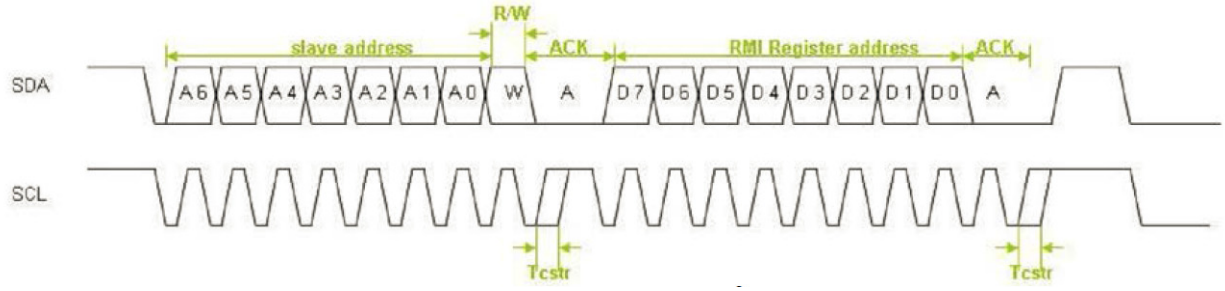

Figure 6. Clock stretching with an I^2C transaction

In-system reprogrammability

The S7885 includes firmware in order to support finger tracking and position reporting. This firmware is stored in non-volatile (flash) memory on-chip and may be updated at any time over the host interface. This capability allows freedom and flexibility when operating with Synaptics devices; simply choose the firmware image that is applicable to your design. Figure 7 illustrates the firmware storage methodology.

Note: Reference code is available from Synaptics that implements the steps for reprogramming the configuration and user interface firmware space.

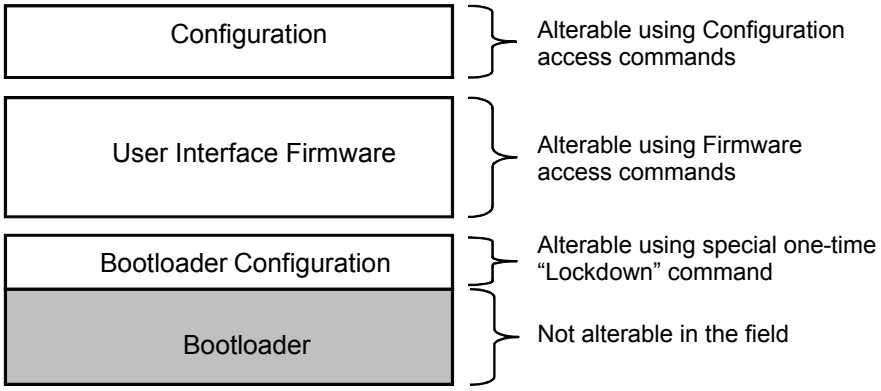

Figure 7. Firmware structure

Configuration

The configuration space stores the default values of the device's control registers. The bootloader provides a mechanism to erase and reprogram this space. Because an existing configuration may not be valid for a new firmware revision, any update to the user interface firmware should be followed by an update of the configuration space.

User interface firmware

The user interface firmware space contains the firmware that implements the primary function of the device. User interface firmware images are provided by Synaptics in an encrypted form to ensure they can only be executed on an appropriate device. It is not possible to erase the user interface firmware space without also erasing the configuration space.

Bootloader configuration

This can be set by a one-time lockdown process when adding user interface firmware for the first time. This permits the same S7885 parts to be deployed in different hosts systems where required bootloader configuration may be different for each.

Bootloader

This is pre-programmed and cannot be changed. The bootloader:

- checks the integrity of the user interface firmware space
- provides the ability to re-flash a new user interface or configuration area.

Electrical specifications

Absolute maximum ratings

Table 6. S7885 absolute maximum ratings

Parameter	Minimum	Maximum	Unit
Voltage on any GPIO pin	–0.3	3.6	V
VDDBUS	–0.3	3.6	V
VDD12	–0.3	1.32	V
VDD18	–0.3	1.98	V
VDDH/VDDHCP	–0.3	3.6	V
Input current at any pin	—	100	mA
Package input current	—	200	mA
Operating temperature	–40	105	°C
Storage temperature, unbiased	–55	125	°C
Lead soldering temperature (10 seconds)	—	260	°C

Note: When the input voltage at any pin exceeds the associated power supply, the current at that pin should be limited to 100 mA. The 200 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 100 mA to two pins. The maximum time this condition can be applied is approximately 10 seconds.

Note: Stresses beyond those listed in Table 6 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: The absolute maximum junction temperature (Tjmax) for this device is 150 °C.

Device level specifications

Table 7. S7885 DC characteristics

Parameter	Symbol	Comment	Minimum	Typical	Maximum	Unit
Analog supply input 1	VDDH	—	2.7	3.3	3.6	V
Analog filter pin 1	VDDRX	Internally filtered power	2.6	—	3.6	V
Analog filter pin 2	VDDA	Internally filtered power	2.6	—	3.6	V
Digital core supply	VDD12	—	1.14	1.2	1.32	V
Analog supply input 2	VDD18	—	1.71	1.8	1.98	V
Internal 1.2V LDO supply input	VDD12LDO	Connect to VDD18	1.62	1.8	1.98	V
Internal 1.8 LDO supply input	VDD18LDO	Connect to VDDH	2.7	—	3.6	V
GPIO power supply	VDDBUS	Shared with VDDH	VDDH	—	VDDH	V
Analog supply input for charge pump and LDO	VDDHCP	Connect to VDDH	2.7	3.3	3.6	V
Positive voltage charge pump output	VDDCP	Typically 2x VDDH	5.4	—	7.2	V
Power supply ripple	—	—	—	—	100	mV (peak-to-peak)

Note: Power supply, even in the presence of non-zero power supply ripple, must remain within the stated minimum and maximum range.

Reliability characteristics

Table 8. S7885 reliability characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Reference Test Method
$FLASH_{DR}$	Flash data retention	10	—	Years	Accelerated test
$FLASH_{ENPB}$	Flash write endurance	1,000	—	Erase/Write Cycles	—
V_{ZAPHBM}(1)	ESD susceptibility HBM	—	± 2	kV	Class 2 (AEC Q100-002/JEDEC JS-001)
V_{ZAPCDM}(1)	ESD susceptibility CDM	—	± 750 corner pins ± 500 all other pins	V	Class C4B (AEC Q100-011)

Note 1: This parameter is tested initially during characterization and after a design or process change that affects the parameter.

GPIO characteristics

Push-pull GPIO characteristics

Table 9. S7885 push-pull GPIO characteristics

Mode	Function	Condition	Input Low Level Voltage (V_{IL}) Maximum (V)	Input High Level Voltage (V_{IH}) Minimum (V)	Input Hysteresis (V_{HYS}) Typical (mV)	Input Capacitance (C_{IN}) Maximum (pF)	Output Voltage Low (V_{OL}) Maximum (V)	Output Voltage High (V_{OH}) Minimum (V)
0	I^2C standard or fast-mode	3.6V ≥ VDDBUS > 2.7V IOL = 3 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4	NA
1	I^2C standard or fast-mode	2.7V ≥ VDDBUS > 1.98V IOL = 3 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4	NA
2	I^2C standard or fast-mode	1.98V ≥ VDDBUS > 1.65V IOL = 3 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.2 x VDDBUS	NA
3	GPIO	3.6V ≥ VDDBUS > 1.65V at 1 MHz IOL = IOH = 20 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4
6	SPI	3.6V ≥ VDDBUS > 1.65V at 17.5 MHz maximum IOL = IOH = 10 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4
6	GPIO	3.6V ≥ VDDBUS > 1.65V IOL = IOH = 10 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4
7	Test	3.6V ≥ VDDBUS > 2.7V IOL = IOH = 30 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4	VDDBUS – 0.4

Open drain GPIO characteristics

Table 10. S7885 open drain GPIO characteristics

Mode	Function	Condition	Input Low Level Voltage (V_{IL}) Maximum (V)	Input High Level Voltage (V_{IH}) Minimum (V)	Input Hysteresis (V_{HYS}) Typical (mV)	Input Capacitance (C_{IN}) Maximum (pF)	Output Voltage Low (V_{OL}) Maximum (V)
0	I^2C standard or fast-mode	3.6V ≥ VDDBUS > 2.7V IOL = 3 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4
1	I^2C standard or fast-mode	2.7V ≥ VDDBUS > 1.98V IOL = 3 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.4
2	I^2C standard or fast-mode	1.98V ≥ VDDBUS > 1.65V IOL = 3 mA	0.3 x VDDBUS	0.75 x VDDBUS	0.05 x VDDBUS	10	0.2 x VDDBUS

Power management

The overall power supply current is a function of the operating power supplies, sleep mode, and product configuration, which can vary significantly. Synaptics measures power consumption as an average current on the power supply pins.

Table 11. Typical power consumption with external VDDH shared with VDDBUS (3.3V), internal VDD18LDO (1.8V), and internal VDD12LDO active (1.2V*)*

Operating Mode	VDDH Current (mA)	VDDBUS Current (µA)	VDDH Power (mW)	VDDBUS Power (mW)	Total Power (mW)
Active – 0 finger	34	0	113	0	113
Active – 1 finger	34	0	113	0	113
Active – 5 fingers	35	0	114	0	114
Active – 10 fingers	35	0	117	0	117
Normal operation	2.6	0	8.5	0	8.5
Sensor sleep	0.37	0	1.2	0	1.2

Note: Measurements are made on a 10.1-inch sensor, 48 receivers and 30 transmitters, VDDH shared with VDDBUS(3.3V), and using RMI over I^2C. Touch report rate at 60 Hz and doze interval at 30 ms.

Timing characteristics

I²C

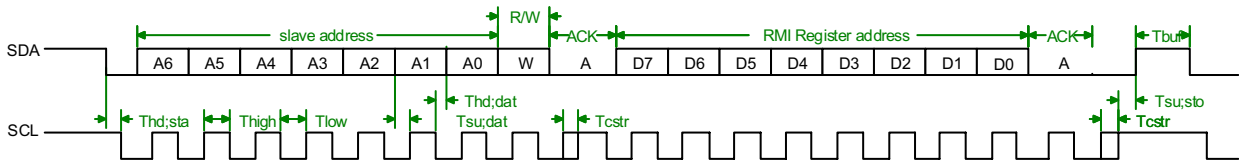

Figure 8. I²C timing

Table 12. I²C parameters

Parameter	Symbol	Standard-Mode			Fast-Mode			Unit
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
SCL clock frequency.	f_{SCL}	—	—	100	—	—	400	kHz
Stretch time.	t_{CSTR}	—	<25	—	—	<25	—	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	—	—	0.6	—	—	µs
LOW period of the SCL clock.	t_{LOW}	4.7	—	—	1.3	—	—	µs
HIGH period of the SCL clock.	t_{HIGH}	4.0	—	—	0.6	—	—	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	—	—	0.6	—	—	µs
Data hold time.	$t_{HD;DAT}$	0	—	3.45	0	—	0.9	µs
Data out valid time.	$t_{VALID;DATO}$	—	—	3.45	—	—	0.9	µs
Data set-up time.	$t_{SU;DAT}$	250	—	—	100	—	—	ns
Rise time of both SDA and SCL signals.	t_r	—	—	1,000	20 + 0.1 C_b	—	300	ns
Fall time of both SDA and SCL signals.	t_f	—	—	300	20 + 0.1 C_b	—	300	ns
Set-up time for STOP condition.	$t_{SU:STO}$	4.0	—	—	0.6	—	—	µs
Bus free time between a STOP and START condition.	t_{BUF}	4.7	—	—	1.3	—	—	µs
Capacitive load for each bus line.	C_b	—	—	400	—	—	400	pF

Power-on sequence and initialization

VDDBUS supplies the communication I/O and GPIOs. VDDH supplies analog power. VDD18 and VDD12 supply the digital IC core power. The S7885 “Power OK” circuitry monitors the VDD18, VDD12, and VDDBUS supply inputs. In order for the POR cycle to commence, the power supplies must start at a lower voltage than the power OK falling threshold and rise monotonically and settle within their tolerances in 25 ms. All three power inputs must be valid before a power on reset condition begins (Figure 9).

The XRESB, external hardware reset input can also be used to force the chip into a reset condition, when the power supply cannot be shut off completely. The VDDBUS power input is provided so that the I^2C bus can remain functional while other power is removed from the touch controller. In this case the VDDBUS power will remain on and other devices that share the I^2C can continue to function. Pull-up resistors on the I^2C bus should be connected to VDDBUS. The SCL and SDA pins are true open-drain I/O pins and will not allow current leakage into the touch controller when the other power rails are switched off. VDDBUS also allows voltage translation with systems using from 1.8V to 3.3V logic.

VDDBUS, VDDH, VDD18, and VDD12 can be powered up in any order. The power state of VDDH is monitored by firmware. The touch controller ATTN interrupt output, typically GPIO PA5, has ESD protection devices that may allow current to leak from the pull-up resistor into the VDDBUS supply, when power is removed. For this reason it is important to connect pull-up resistors to the VDDBUS supply (and not other supplies). Another reason is that if VDDBUS and VDD18 are combined, the leakage current from the pull-up resistor may prevent the VDD18 from decaying fast after power is removed. And much time will be required for the voltage to decay low enough for the POR cycle to function normally.

When powering the S7885 up or down, system design should ensure that the voltages on the signal pins in Table 6 are observed. Failure to follow this requirement may lead to unreliable operation of, or damage to, the device. Open-drain signals (for example: SCL/PA9 and SDA/PA8) are high-impedance at power-up and will transition high when the external pull-ups power (VDDBUS) is applied.

During the initialization phase ($T_{powerup}$), the touch controller reset and firmware initialization routines may take up to 45 ms. During this time, the ATTN signal will be de-asserted and no host commands will be recognized. After the touch controller is fully initialized, the ATTN pin will be asserted and host communication is enabled.

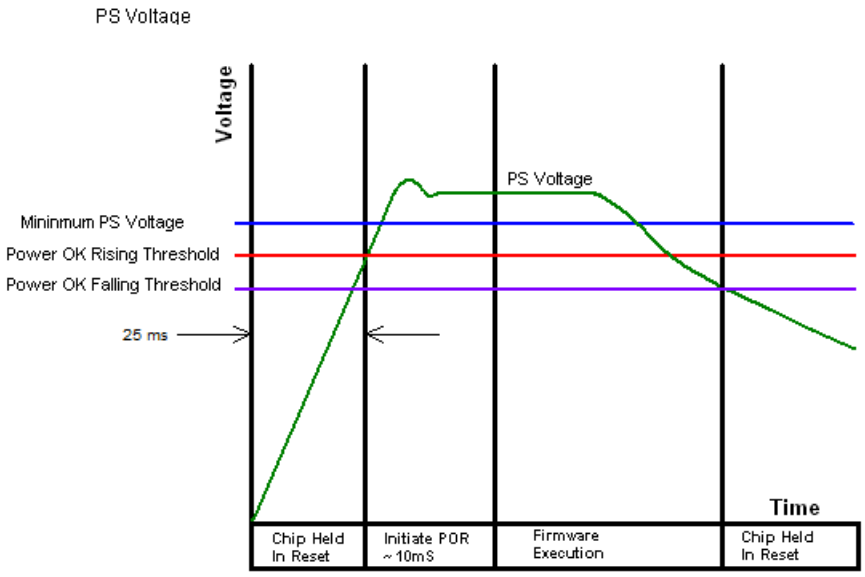

Figure 9. Power supply power-on sequence and start firmware execution

Power supply sequencing

The power supplies must start at below the power OK falling threshold and rise monotonically to their specified tolerance within 25 ms. Thereafter they must stay within the permitted tolerance. During power up when all power inputs are valid, I/O pin PA3 is driven high by the touch controller and will remain high until the hardware power on reset timer expires (minimum of 5 ms, maximum of 21 ms) at which time pin PA3 will pulse low. In systems where pin PA3 is used, the host should expect this power up pulse behavior. If this behavior is not tolerable, other GPIO pins should be used instead.

Important: It is strongly recommended to power-up the touch subsystem last in a device. Doing so allows the touch controller to measure its baseline with other subsystems (such as an LCD) powered on, enabling optimized performance.

Table 13. Power OK characteristics

Power Supply	Power OK Rising Threshold	Power OK Falling Threshold	Power Supply Minimum Voltage	Unit
VDD12	1.08	1.02	1.14	V
VDD18	1.62	1.53	1.71	V
VDDBUS	1.62	1.53	1.71	V

Power-on interface timing

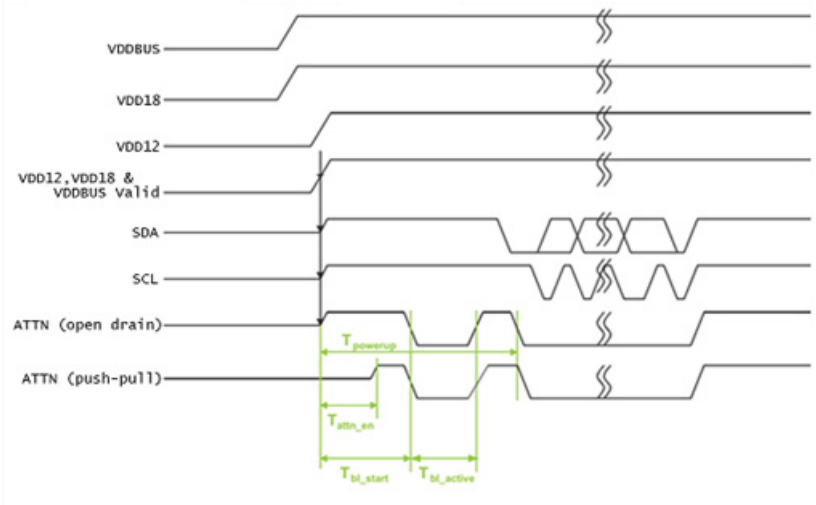

Figure 10. Power-on interface timing diagram

Table 14. Power-on sequence and external reset timing

Power Supply	Minimum	Maximum	Unit
T_{attn_en}	5	21	ms
$T_{powerup}$	—	45	ms
T_{bl_start} (bootloader start)	—	30	ms
T_{bl_active} (bootloader active)	—	15	ms
T_{reset} (XRESB pin)	100	—	ns

External reset timing

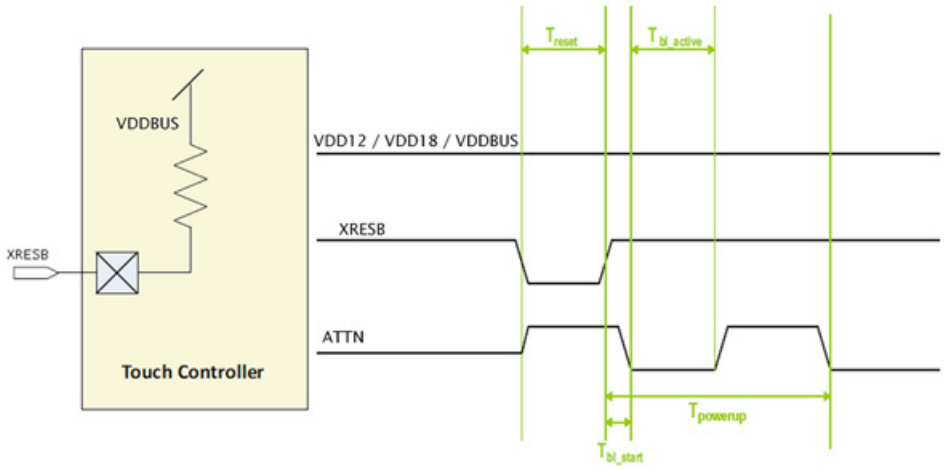

Figure 11. External reset timing diagram

Package and ordering information

Package drawing

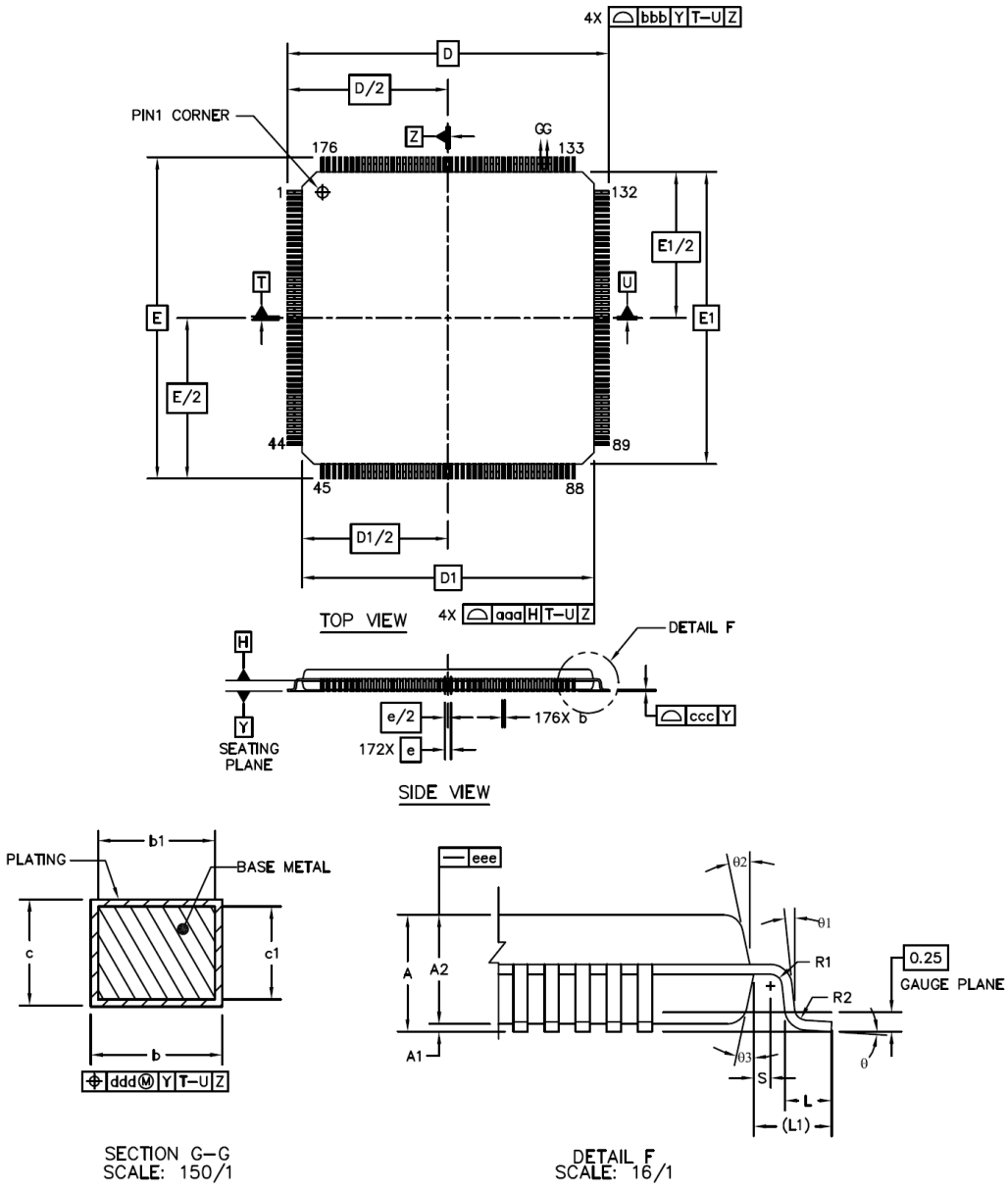

Figure 12. S7885 package drawing

Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane datum H.

Note 2: Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

Dimensions

All measurements are in millimeters unless otherwise specified.

Table 15. 176LQFP dimensions

Aspect		Symbol	Common Dimensions		
			Minimum	Typical	Maximum
Total thickness		A	—	—	1.6
Stand off		A1	0.05	—	0.15
Mold thickness		A2	1.35	1.4	1.45
Lead width (plating)		b	0.13	0.18	0.23
Lead width		b1	0.13	0.16	0.19
L/F thickness (plating)		c	0.09	—	0.2
L/F thickness		c1	0.09	—	0.16
Body size	X	D	—	22 BSC	—
	Y	E	—	22 BSC	—
	X	D1	—	20 BSC	—
	Y	E1	—	20 BSC	—
Lead pitch		e	—	0.4 BSC	—
		L	0.45	0.6	0.75
Footprint		L1	—	1 REF	—
		θ	0°	3.5°	7°
		θ1	0°	—	—
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	—	—
		R2	0.08	—	0.2
		S	0.2	—	—
Package edge tolerance		a a a	—	0.1	—
Lead edge tolerance		b b b	—	0.2	—
Coplanarity		c c c	—	0.08	—
Lead offset		d d d	—	0.07	—
Mold flatness		e e e	—	0.05	—

Package marking

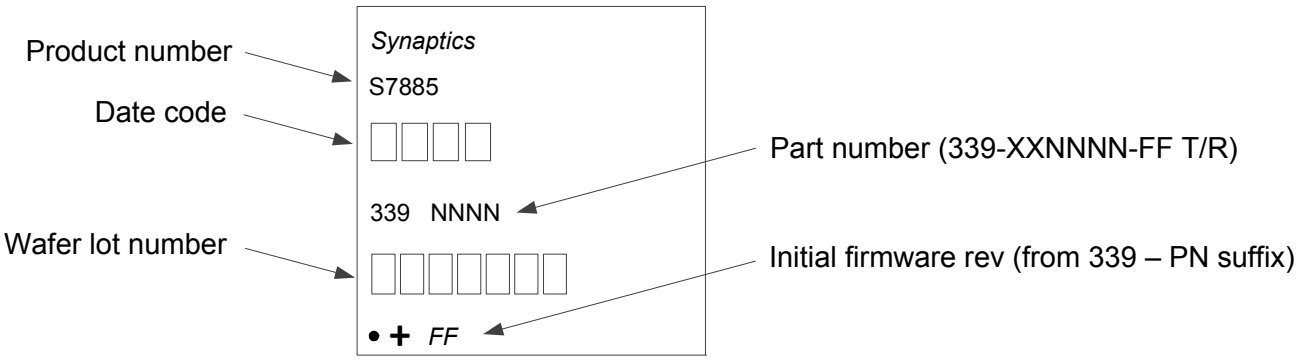

Figure 13. S7885 package marking

Ordering information

Refer to the *Touch Controller Ordering Guide* (PN: 511-000481-01) for details.

Shipment packaging

The S7885 can be shipped either in trays or in tape-and-reel packaging.

For information about tape-and-reel packaging, see the *ASIC Tape-and-Reel Package Specification* (PN: 528-000187-01).

For tray packaging specifics, please contact Synaptics.

Environmental and regulatory compliance

This Synaptics product is built in compliance with the RoHS directive and the *Synaptics Quality Specification: Environmental Conservation Program* (PN: 526-000223-01). This Synaptics product is also Halogen-Free (HF) compliant.

Reference documents

- *ASIC Tape-and-Reel Package Specification* (PN: 528-000187-01)
- *ClearPad Integration Guide* (PN: 511-000399-01)
- *ClearPad Sensor Design Guidelines* (PN: 511-000384-01)
- *Synaptics Quality Specification: Environmental Conservation Program* (PN: 526-000223-01)
- *Synaptics RMI4 Specification* (PN: 511-000405-01)
- *Touch Controller Ordering Guide* (PN: 511-000481-01)

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Notice

Revision history

Table 16. Revision history

Revision	Description
A	Updated Features and Benefits section and Push-Pull GPIO Characteristics table.
B	Updated Transmitter and Receiver Configurations (Table 2), Configuration Pin Options (Table 3), and GPIO Characteristics (Table 9 and Table 10).

Contact us

To locate the Synaptics office nearest you, visit our website at www.synaptics.com.